AMENDMENTS TO THE CLAIMS

Please amend claims 1, 3-4 and 6 as follows:

1. (currently amended) A method for fabricating a merged logic device, comprising:

forming a high voltage p-type well region and a logic region on a ~~high voltage device forming region of a~~ semiconductor substrate ~~and on the semiconductor substrate~~;

simultaneously conducting an ion implantation for forming a logic p-type well region on the logic region and a high voltage n-type well region on the high voltage p-type well region;

forming a high voltage gate oxide film on the resulting structure and conducting a threshold voltage ion implantation process;

forming a logic gate oxide film on the logic region and ~~simultaneously~~ forming a logic gate electrode on the logic region and a high voltage gate electrode on the high voltage ~~device forming~~ p-type well region;

forming a logic double diffused drain (DDD) region on the logic region and forming spacers on sides of the logic gate ~~electrodes~~ electrode and the high voltage gate electrode; and

forming logic source/drain regions, high voltage source/drain regions and a bulk bias control region.

2. (original) The method of claim 1, wherein a field stop layer is formed simultaneously with the formation of the logic p-type well region.

3. (currently amended) The method of claim 1, wherein a portion of the high voltage gate oxide film disposed over ~~formed on~~ the logic region is removed by a wet etching process and a logic gate oxide film is formed over the logic region.

4. (currently amended) A method for fabricating the merged logic device comprising:

forming a high voltage p-type well region ~~on a high voltage device forming region of~~ and a logic region on a semiconductor substrate~~, the semiconductor substrate also having a logic region~~;

~~simultaneously~~ conducting an ion implantation for forming a p-type well region on the logic region ~~of the semiconductor substrate~~ and a high voltage n-type well region on the high voltage p-type well region;

forming a high voltage gate oxide film on the resulting structure;

conducting a threshold voltage ion implantation process;

forming a logic gate oxide film on the logic region;

~~simultaneously~~ forming a logic gate electrode on the logic region and a high voltage gate electrode on the high voltage p-type well ~~device forming~~ region;

forming a logic DDD region on the logic region;

forming spacers on side of the logic gate electrode and the high voltage gate electrode; and

forming logic source/drain regions, high voltage source/drain regions and a bulk bias control region.

5. (original) The method of claim 4 wherein a field stop layer is formed simultaneously with the formation of the logic p-type well region.

6. (currently amended) The method of claim 4 wherein a portion of the high voltage gate oxide film formed on the logic region is removed by a wet etching process and a logic gate oxide film is subsequently formed on the logic region.